REMARKS

1. In response to the Office Action mailed March 12, 2004, Applicants respectfully requests reconsideration. Claims 1-4, 6 and 11-15 were last presented for examination. All claims were rejected in the outstanding Office Action. In the foregoing Amendments, claims 1-4, 6 and 11-15 have been cancelled and replaced with new claims 16-44. Thus, upon entry of this paper, claims 16-44 will be pending in this application. These Amendments are believed not to introduce new matter and their entry is respectfully requested.

2. Applicants acknowledge the additional reference made of record in Form PTO-892 attached to the outstanding Office Action.

3. In the Office Action Summary sheet it is noted that the specification was objected to by the Examiner. However, there is no detailed description of an objection to the specification presented in the Detailed Action. Accordingly, Applicants believe the Summary sheet is incorrectly marked, and no amendments and/or arguments regarding the specification are presented herein.

4. Applicants note with appreciation the Examiner's acceptance of the formal drawings filed on 25 November 2000.

5. The claim objections are rendered moot due to the cancellation of the pending claims.

6. Because of certain apparent misunderstandings on the part of the examiner with regard to source synchronous links, described below, Applicants have replaced all claims with new claims which more clearly articulate the inherent features of a source synchronous link. Such recitations simply make explicit that which is implicit in the now-canceled claims.

7. Independent claim 1 and dependent claims 2-3 have been rejected under 35 U.S.C. §103(a) as being anticipated by National Semiconductor DS26C31T/DS26C31M CMOS Quad TRI-STATE Differential Line Driver (hereinafter, "National") in view of Texas-'111 and in further view of Texas Instruments CDC328A 1-Line to 6-Line Clock Driver with Selectable Polarity (hereinafter, "Texas-'328A). Independent claim 4 and dependent claim 6 have been rejected under 35 U.S.C. §102(b) as being anticipate by Texas Instruments CDC111 1-Line to 9-Line differential LVPECL Clock Driver (hereinafter, "Texas-'111"). Independent claim 11 and dependent claims 12-15 have been rejected under 35 U.S.C. §102(a) as being anticipated by U.S. Patent Application 6,026,051 to Keeth, *et al.*

(hereinafter, "Keeth"). Applicants respectfully disagree, and assert that these references, taken alone or in combination, neither disclose, teach or suggest Applicants' invention as recited in the new independent claims set forth in this paper.

8. First, the Examiner has apparently disregarded the fact that the present invention as claimed is directed to methods and apparatus for a source synchronous link and associated communications. As is well-known in the art, a source synchronous link is often implemented to overcome problems associated with common-clocked data transfer systems. "In a source synchronous link clock or strobe signals are sent between components along with the data signals to communicate timing information. Instead of having one or more components operate on a common clock signal, data is communicated at a speed that is not set by a common clock signal. The strobe signal sent with the data may be used, for example, to start an internal clock, for latching of the data, or for other timing purposes." (*See*, Applicants' application, pg. 2, lns. 6-15.) The Examiner has failed to rely on a reference that, when taken alone or in combination with other references of record, teaches or suggests a source synchronous link or halting a data strobe in a source synchronous link as claimed. For at least this reason, Applicants submit that new claims 16-44 are patentable over the art of record.

9. Second, the Examiner has not properly interpreted recited features of Applicants' claimed invention. Specifically, the Examiner notes in the Response to Arguments section of the Office Action, that "the term "data strobe signal" does not limit the claim to anything other than digital "data." This reading of Applicants' claim is improper. As noted above, a clock signal is transmitted with the data in a source synchronous link. Throughout Applicants' application, the term "data strobe signals" refers to clock signals transmitted over the source synchronous link: "The clock signal that is transmitted with the data signals is referred to as a data strobe..." (*See*, Applicants' application, pg. 10, lns. 5-7.) Thus, in contrast to the Examiner's assertion, a data strobe signal is a clock signal that is transmitted over a source synchronous link. As is clear from this present Office Action, the Examiner has relied on this misplaced interpretation in the prior rejections. For at least this reason, Applicants submit that new claims 16-44 are patentable over the art of record.

10. Third, the Examiner has failed to apply the proper standards of patentability in the current Office Action. In the Response to Arguments section of the Action, the Examiner asserts that "the logic circuits of National are perfectly suited for the reception of and

generation of data strobe signals." Beyond the above-noted improper reading of the term "data strobe signal," Applicants assert that the "suitability" of the National Differential Line Driver to perform a particular operation is not a legitimate basis for rejecting a claim. "Suitability" does not mean the reference teaches or suggests that which is recited in Applicants' claims. For at least this reason, Applicants submit the rejections are improper, and that new claims 16-44 are patentable over the art of record.

11. With regard to Texas-'111 and Texas-'328A, these references teach nothing more than a clock driver that distributes one pair of differential clock inputs to six and nine pairs of differential clock outputs, respectively. Such drivers are used to distribute a clock through a circuit board or system. As noted in the Background of the Invention Section of Applicants' application, "[t]ypically, with regard to chipsets, an external clock chip generates a system clock that is routed throughout the circuit board to different components for translation into an internal clock." The source synchronous link overcomes potential drawbacks of distributing a system clock, as noted in Applicants' application. (*See*, Applicants' application, pg. 1, ln. 21- pg. 2, ln. 15.) The Texas-'111 and Texas-'328A clock drivers are used for distributing a system clock. Thus, whether taken alone or in combination, Texas-'111 and Texas-'328A neither disclose, teach nor suggest transmitting clock or data strobe signals over a source synchronous link as recited in Applicants' new claims 16-44.

12. With regard to National, Applicants refer the Examiner to the above discussion regarding the improper reliance on the suitability of a device in making a rejection. In addition, the Examiner improperly asserts that National discloses a source synchronous link comprising a communication link, and a source synchronous receiver and transmitter coupled to the communication link. In contrast, National teaches a quad differential line driver for transmitting digital data over balanced lines. There is no mention whatsoever in National of a source synchronous link, nor is there any teaching or suggestion that National be implemented as a source synchronous transmitter or receiver as claimed. In fact, National does not receive, buffer or otherwise process or generate data strobe signals. Taking the logic diagram illustrated on page 4, each of the four drivers are used to transmit data, not data strobes. In fact, a careful review of the input and output signals illustrated on page 1 of National will reveal that the device does nothing more than buffer the noted TTL or CMOS data input levels and translates these to RS-422 output levels. (*See*, National, General Description, para. 2.) National, therefore, fails to disclose, teach or suggest the transmission

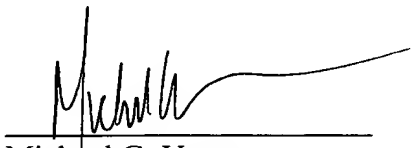
of data signals and data strobe signals over a source synchronous communication link as recited in new claims 16-44.

13. With regard to Keeth, the Examiner asserts that Keeth discloses a differential data strobe signal generator as claimed, referring Applicants to elements 38, 40, 46 and 48, and Figure 3 of Keeth. In the Response to Arguments section of the Action, the Examiner also notes that Keeth clearly shows transmit logic to generate a differential data strobe, referring to the DCLK0OUT and DCLK0OUT* signals configured to "transmit" internal to the RAM. However, Keeth neither discloses, teaches nor suggests halting of data strobes over a source synchronous link. The lack of such teaching is revealed in the rejections based on Keeth in which reliance is made on transmissions between Keeth's memory controller and SLDRAM in combination with transmissions that occur elsewhere in the Keeth system, namely transmissions internal to the SLDRAM. For at least this reason, Keeth neither discloses, teaches nor suggests Applicants' invention as recited in new claims 16-44.

14. The dependent claims are patentable for at least the same reasons as those noted above in connection with their respective base claims.

15. In view of the foregoing, this application should be in condition for allowance. A notice to this effect is respectfully requested.

Respectfully submitted,



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May 12, 2004